AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 7-10 as shown below.

The following is a complete list of all claims in this application.

1. (Previously Presented) A liquid crystal display, comprising:

a timing controller receiving image signals and synchronization signals, and generating control signals;

a gate driver sequentially applying a stepped-wave pattern gate voltage to a plurality of gate lines, the stepped-wave pattern gate voltage including a reset interval for converting a grayscale level of a first liquid crystal capacitor connected to a subsequent gate line through a first thin film transistor to a first extreme grayscale level, a gate-on interval, and an overshoot interval following the gate-on interval and having the polarity of a data voltage; and

a data driver for applying the data voltage to the second liquid crystal capacitor of the liquid crystal panel according to the control signals of the timing controller.

2. (Previously Presented) The liquid crystal display of claim 1, wherein the first extreme grayscale level is a black grayscale level when in a normally white mode.

3. (Previously Presented) The liquid crystal display of claim 1, wherein the first extreme grayscale level is a white grayscale level when in a normally black mode.

4. (Cancelled)

5. (Previously Presented) A drive method for a liquid crystal display, comprising:

sequentially applying a stepped-wave pattern gate voltage to the gate lines, the stepped-wave pattern gate voltage including a reset interval for converting a grayscale level of a first liquid crystal capacitor connected to a subsequent gate line through a first thin film transistor to a first extreme grayscale level, a gate-on interval, and an overshoot interval following the interval and having the polarity of a data voltage; and

applying the data voltage to the second liquid crystal capacitor of the liquid crystal panel.

6. (Cancelled)

7. (Currently Amended) The method of claim ~~6~~5, wherein the gate voltage in the reset interval is identical in polarity to a polarity of the gate voltage in the overshoot interval.

8. (Currently Amended) The method of claim ~~6~~5, wherein the gate voltage in the reset interval is opposite in polarity to a polarity of the gate voltage in the overshoot interval.

9. (Currently Amended) The method of claim ~~6~~5, wherein the gate voltage in the overshoot interval is +3V to +10V relative to a gate-off voltage.

10. (Currently Amended) The method of claim ~~6~~5, wherein the overshoot interval starts at a point where the gate-on interval ends, and converts to a gate-off voltage at a position where the gate-on interval doubles.

11. (Previously Presented) The method of claim 5, wherein the first extreme grayscale level is a white grayscale level when in a normally black mode.

12. (Previously Presented) The method of claim 5, wherein the first extreme grayscale level is a black grayscale level when in a normally white mode.

13. (Previously Presented) The method of claim 5, wherein the gate voltage in the reset interval is +3V to +10V relative to a gate-off voltage.

14. (Previously Presented) The method of claim 5, wherein a starting point of the reset interval is within about 0.5 μs to about 5 μs from a starting point of the gate-on interval.

15. (Previously Presented) A liquid crystal display, comprising:

first and second gate lines sequentially supplied with a gate signal;

a data line for transmitting a first data voltage and a second data voltage;

a first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage;

a second switching element connected to the second gate line and the data line and selectively transmitting the second data voltage;

a first liquid crystal capacitor connected to the first switching element;

a second liquid crystal capacitor connected to the second switching element;

a storage capacitor connected between the second liquid crystal capacitor and the first gate line;

a data driver applying the first and the second data voltages to the data line; and

a gate driver sequentially applying the gate signal to the first and the second gate lines,

wherein the gate signal has first, second, third, and fourth voltages during sequentially arranged first, second, third, and fourth time intervals, respectively.

16. (Previously Presented) The liquid crystal display of claim 15, wherein the first switching element and the second switching element turn on by the second voltage and turn off by the fourth voltage.

17. (Previously Presented) The liquid crystal display of claim 16, wherein the first liquid crystal capacitor and the second liquid crystal capacitor are supplied with a common voltage, the third voltage of the gate signal applied to the first gate line is higher than the fourth voltage when the first data voltage is higher than the common voltage, and the third voltage of the gate signal applied to the first gate line is lower than the fourth voltage when the first data voltage is lower than the common voltage.

18. (Previously Presented) The liquid crystal display of claim 17, wherein both the first and the third voltages are higher or lower than the fourth voltage.

19. (Previously Presented) The liquid crystal display of claim 18, wherein the liquid crystal display operates in normally white mode.

20. (Previously Presented) The liquid crystal display of claim 17, wherein one of the first and the third voltages is higher than the fourth voltage and the other of the first and the third voltages is lower than the fourth voltage.

21. (Previously Presented) The liquid crystal display of claim 20, wherein the liquid crystal display operates in normally black mode.

22. (Previously Presented) The liquid crystal display of claim 16, wherein both the first and the third voltages are higher or lower than the fourth voltage.

23. (Previously Presented) The liquid crystal display of claim 22, wherein the third voltage has a value between the first voltage and the fourth voltage.

24. (Previously Presented) The liquid crystal display of claim 16, wherein one of the first and the third voltages is higher than the fourth voltage and the other of the first and the third voltages is lower than the fourth voltage.

25. (Previously Presented) A liquid crystal display, comprising:

first and second gate lines sequentially supplied with a gate signal;

a data line transmitting a first data voltage and a second data voltage;

a first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage;

a second switching element connected to the second gate line and the data line and selectively transmitting the second data voltage;

a first liquid crystal capacitor connected between the first switching element and a common voltage;

a second liquid crystal capacitor connected between the second switching element and the common voltage;

a storage capacitor connected between the second liquid crystal capacitor and the first gate line;

a data driver applying the first and the second data voltages to the data line; and

a gate driver sequentially applying the gate signal to the first and the second gate lines,

wherein the gate signal has first, second, and third voltages during first, second, and third time intervals, respectively, and the first voltage turns on the first and the second switching elements and the second voltage turns off the first and the second switching elements, the third interval precedes the first time interval, and a polarity of the third voltage with respect to the second voltage is the same as a polarity of the data voltage with respect to the common voltage.

26. (Previously Presented) The liquid crystal display of claim 25, wherein the gate signal further has a fourth voltage, which has a polarity with respect to the second voltage equal to the polarity of the data voltage, during a fourth time interval following the first time interval.